Amendments to the Specification

The paragraph on Page 1, starting at line 4, is amended as follows:

This application is a continuation of U.S. Patent Application Serial No. 10/131,963, filed April 25, 2002, now U.S. Patent No. 6,657,503, which is a continuation of U.S. Patent Application Serial No. 09/507,114, filed February 17, 2000, now U.S. Patent No. 6,414,557.

The paragraph on Page 9, starting at line 2, is amended as follows:

Figure 5 shows the details of a differential delay circuit 410 of the VCO [[vr¢o]] circuit 400 in accordance with a preferred embodiment of the invention. The differential delay circuit 410 provides a relatively high level of isolation from noise originating from both the voltage supply and ground. Consequently, the VCO output signal VCO_out has a reduced amount of jitter in the presence of such noise. In this embodiment, the differential delay circuit 410 is implemented using CMOS technology. In alternative embodiments of the invention, however, the differential delay circuit 410 may be implemented using other technologies such as silicon bipolar and GaAs HBT.